PCI/PXI-9816/26/46

4-CH 16-Bit 10/20/40 MS/s Digitizer
with 512 MB SDRAM
User's Manual

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1 Introduction

The ADLINK PCI/PXI-9816/26/46 are 10 MS/s, 20 MS/s, and 40 MS/s sampling 16-bit 4-CH digitizers designed for digitizing high frequency and wide dynamic range signals with an input frequency up to 20 MHz. The analog input range can be programmed via software to ±1 V or ±0.2 V. With deep onboard acquisition memory up to 512 MB, the PCI/PXI-9816/26/46 are not limited by the data transfer rate of the PCI bus to enable the recording of waveforms for extended periods of time.

The PCI/PXI-9816/26/46 are equipped with four high linearity 16-bit A/D converters ideal for demanding applications with a high dynamic range such as radar, ultrasound, and software-defined radio.

Analog Input

The PCI/PXI-9816/26/46 each feature four analog input channels. The bandwidth of each channel can be up to 5 MHz, 10 MHz, and 20 MHz for PCI/PXI-9816, PCI/PXI-9826, and PCI/PXI-9846, respectively. The input ranges are software programmable as either ±1 V or ±0.2 V. Software selectable 50 Ω input impedance makes it easy to interface with high-speed, high-frequency signals.

Acquisition System and On-board Memory

The PCI/PXI-9816/26/46 include four 16-bit A/D converters to digitize the input signals. These four channels sample signals simultaneously at a maximum sampling rate of 10 MS/s, 20 MS/s, and 40 MS/s, respectively. The PCI/PXI-9816/26/46 supports a total of 512 MB on-board memory. The digitized data is stored in the on-board memory before being transferred to the host memory. The data transfer is performed using scatter-gather DMA, which provides a high data throughput rate and uses system memory more effectively. If the data throughput from digitizer is less than the available PCI bus bandwidth, the PCI/PXI-9816/26/46 also features an on-board 2 K-sample FIFO to achieve real-time transfer directly to the host memory by bypassing the on-board memory.

Flexible Triggering

The PCI/PXI-9816/26/46 feature flexible triggering options such as a software trigger, external digital trigger, an analog trigger from any of the analog input channels and triggers from the PXI trigger bus. These versatile trigger sources allow you to configure the PCI/PXI-9816/26/46 to fit your application needs. Post-trigger, delay-trigger, pre-trigger and middle-trigger modes are also available to acquire data around the trigger event. The PCI/PXI-9816/26/46 also features repeated trigger acquisition, so you can acquire data in multiple segments with successive trigger events at extremely short rearming intervals.

Multiple-Module Synchronization

The versatile trigger options provided by the PXI backplane allow the PCI/PXI-9816/26/46 to achieve multi-module synchronization in a simplified way. Utilizing the PXI Trigger bus, the PCI/PXI-9816/26/46 can output trigger signals and the timebase to the PXI trigger bus when configured as a master, or receive trigger signals and the timebase from the PXI trigger bus when configured as a slave. Moreover, when the PCI/PXI-9816/26/46 is plugged into a peripheral slot of a PXI system, they can also receive triggers or the timebase from the PXI star trigger controller slot. The precision 10 MHz clock that comes from the PXI backplane can also be used as one of the timebase sources. Combining these PXI trigger features with the interface of the PCI/PXI-9816/26/46 makes it very easy to synchronize multiple modules.

Calibration

The PCI/PXI-9816/26/46 include a precision on-board reference with very low temperature drift. This feature not only provides a stable calibration source for auto-calibration but also maintains stable acquisition accuracy over a wide temperature range. The automated calibration process can be done through software without need for any manually adjustments. Once the calibration process has completed, the calibration information will be stored in the on-board EEPROM so that the values can be loaded and used as needed by the board.

1.1 Features

- 3U Eurocard form factor (PXI version)
- Standard height, half-length PCI form factor (PCI version)
- Support 5 V and 3.3 V PCI signaling
- Support 32-bit / 66 MHz PCI interface
- 4 channels simultaneous single-ended analog input
- 16-bit high resolution ADC
- Up to 10 MS/s, 20 MS/s and 40 MS/s per channel
- 512 MB onboard memory for data storage
- Software selectable 50 Ω or 1 MΩ input impedance
- Programmable input voltage range: ±0.2V/±1V or ±1V/±5V
- 5 MHz, 10 MHz and 20 MHz analog input bandwidth for PCI/PXI-9816, PCI/PXI-9826 and PCI/PXI-9846, respectively
- Multiple modules synchronization through PXI trigger bus
- Support scatter gather DMA transfer
- Fully auto calibration
- 90 dBc SFDR, 79 dBc SINAD and 12.8-bit ENOB (PXI-9816)

1.2 Applications

- Software radio/wireless communication
- Radar/Sonar/Lidar
- Ultrasound
- Imaging
- Military/Laboratory/Research

1.3 Specifications

Analog Input

Specification	Value
Number of Channels	4 single-ended channels
Input Connector	BNC
Input Impedance	50 Ω or 1 MΩ, software selectable, default 50Ω
Input Coupling	DC
Input Range	(±0.2V, ±1V) or (±1V, ±5V), software selectable
Overvoltage Protection	±5V for (±0.2V, ±1V) ±15V for (±1V, ±5V)
ADC Resolution	16-Bit, 1 in 65536
Crosstalk	≤-80 dB at 1MHz, for all input ranges at 50 Ω input impedance

Table 1-1: Analog Input Specifications

Offset Error				
Model Name	PXI-9816D PXI-9826D PXI-9846D PXI-9846W PCI-9846D		PXI-9846H, PCI-9816H PCI-9826H PCI-9846H	
Offset Error	±0.2 mV		±0.3 mV	
Gain Error				
Input Range	±0.2 V	±1 V	±1 V	±5 V
Gain Error	±0.1%	±0.05%	±0.1%	±0.06%
Note: When calculating offset error and gain error, sampled data are averaged with 65536 points and AI channel configured with 50 Ω input impedance.				

Table 1-2: Offset and Gain Error

-3dB Bandwidth, typical				
Input Range	PXI-9816D	PXI -9826D	PXI-9846D PCI-9846D	PXI-9846W
±0.2 V, ±1 V	5.1MHz	9.6MHz	20MHz	80MHz (±1 V) 50MHz (±0.2 V)
Input Range	PCI-9816H	PCI-9826H	PXI-9846H PCI-9846H	---
±1 V, ±5 V	5.1MHz	9.6MHz	20MHz	---

Table 1-3: -3dB Bandwidth, typical

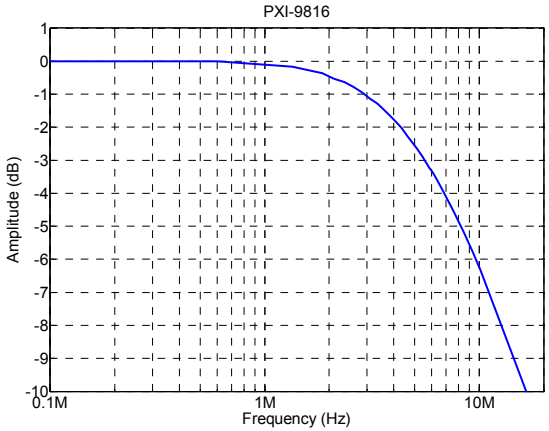

Figure 1-1: PCI/PXI-9816 Bandwidth Chart

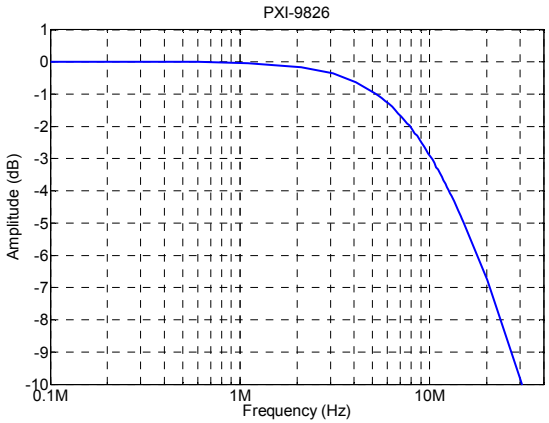

Figure 1-2: PCI/PXI-9826 Bandwidth Chart

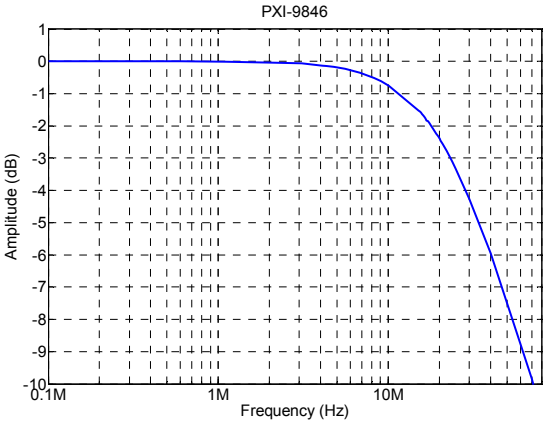

Figure 1-3: PXI-9846 Bandwidth Chart

System Noise (measured and calculated under 50 Ω input impedance)					
Input Range	PXI-9816D	PXI-9826D	PXI-9846D	PXI-9846W	PCI-9846D
±0.2 V	5.0 LSB_{RMS}	6.0 LSB_{RMS}	8.0 LSB_{RMS}	15.0 LSB_{RMS}	8.0 LSB_{RMS}
±1 V	3.0 LSB_{RMS}	4.0 LSB_{RMS}	5.0 LSB_{RMS}	7.0 LSB_{RMS}	5.0 LSB_{RMS}
Input Range	PCI-9816H	PCI-9826H	PCI-9846H	PXI-9846H	
±1 V	5.0 LSB_{RMS}	6.0 LSB_{RMS}	8.0 LSB_{RMS}	8.0 LSB_{RMS}	
±5 V	3.0 LSB_{RMS}	4.0 LSB_{RMS}	5.0 LSB_{RMS}	5.0 LSB_{RMS}	

Table 1-4: System Noise

Spectral Characteristics – PXI-9816

Specification	Input Range	
	±1 V	±0.2 V
Signal to Noise and Distortion (SINAD), typical	79.11 dBc	75.93 dBc
Signal-to-Noise Ratio (SNR), typical	79.36 dBc	75.96 dBc
Total Harmonic Distortion (THD), typical	-89.90 dBc	-95.77 dBc
Spurious Free Dynamic Range (SFDR), typical	90.37 dBc	98.65 dBc
Effective Number of Bit (ENOB), typical	12.85-Bit	12.32-Bit
Test Conditions: Input signal frequency is 0.998 MHz. Digitizer sampling rate at 10 MHz with 50 Ω input impedance. Calculated with 64 K-point data. Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.		

Table 1-5: Spectral Characteristics – PCI/PXI-9816

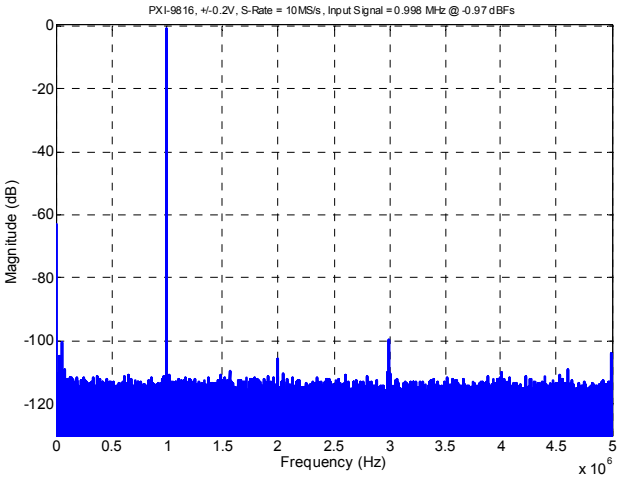

Figure 1-4: PXI-9816 FFT with ±0.2 V Input Range

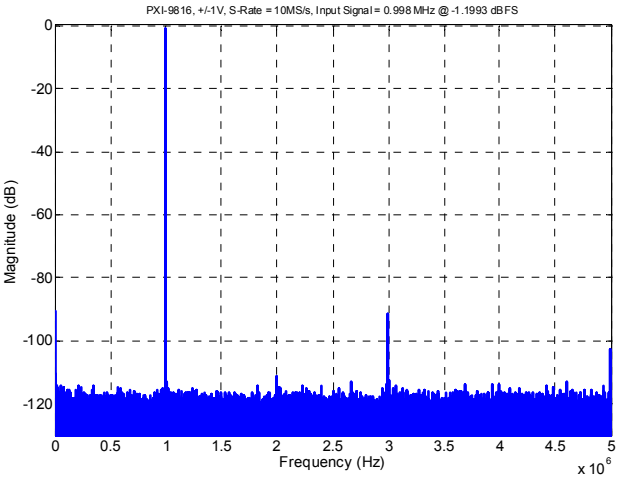

Figure 1-5: PXI-9816 FFT with ±1 V Input Range

Spectral Characteristics – PXI-9826

Specification	Input Range	
	±1 V	±0.2 V
Signal to Noise and Distortion (SINAD), typical	78.63 dBc	74.44 dBc
Signal-to-Noise Ratio (SNR), typical	79.95 dBc	74.48 dBc
Total Harmonic Distortion (THD), typical	-88.29 dBc	-93.52 dBc
Spurious Free Dynamic Range (SFDR), typical	88.88dBc	95.52 dBc
Effective Number of Bit (ENOB), typical	12.77-Bit	12.07-Bit
Test Conditions: Input signal frequency is 0.998 MHz. Digitizer sampling rate at 20 MHz with 50 Ω input impedance. Calculated with 64 K-point data. Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.		

Table 1-6: Spectral Characteristics – PXI-9826

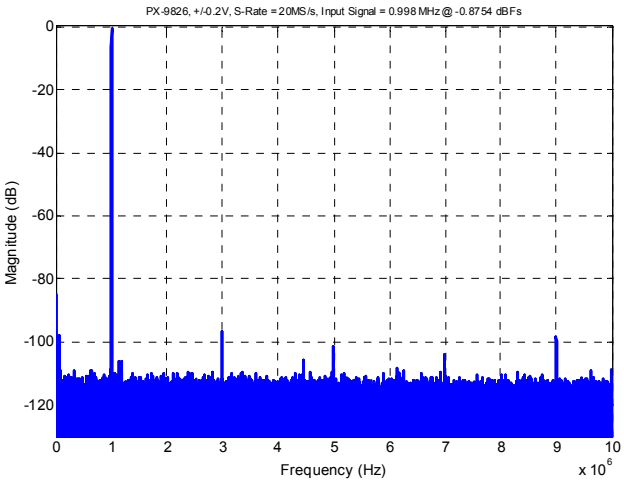

Figure 1-6: PXI-9826 FFT with ±0.2 V Input Range

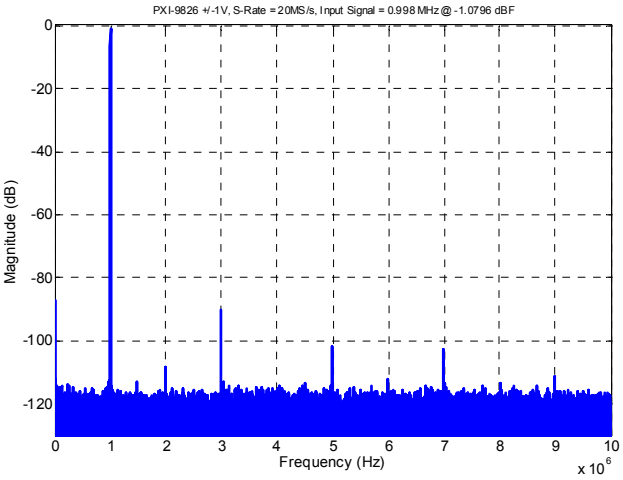

Figure 1-7: PXI-9826 FFT with ±1 V Input Range

Spectral Characteristics – PXI-9846

Specification	Input Range	
	±1 V	±0.2 V
Signal to Noise and Distortion (SINAD), typical	76.06 dBc	71.97 dBc
Signal-to-Noise Ratio (SNR), typical	76.17 dBc	71.98 dBc
Total Harmonic Distortion (THD), typical	-90.65 dBc	-95.78 dBc
Spurious Free Dynamic Range (SFDR), typical	91.62 dBc	96.15 dBc
Effective Number of Bit (ENOB), typical	12.34-Bit	11.66-Bit
Test Conditions: Input signal frequency is 0.998 MHz. Digitizer sampling rate at 40 MHz with 50 Ω input impedance. Calculated with 64 K-point data. Note that these dynamic parameters may vary from one unit to another, with input frequency and with the full scale input range selected.		

Table 1-7: Spectral Characteristics – PCI/PXI-9846

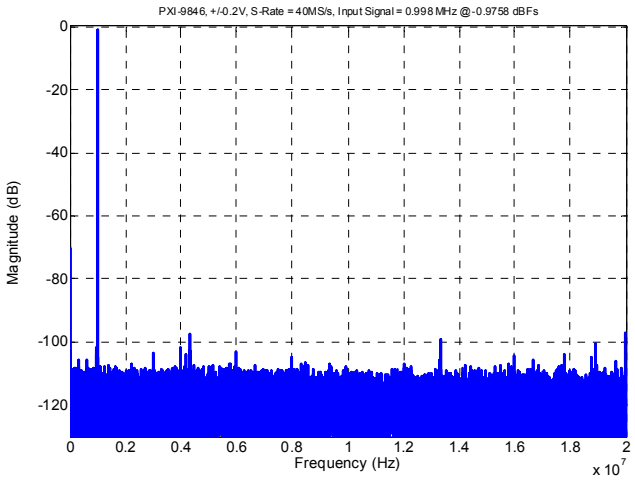

Figure 1-8: PXI-9846 FFT with ±0.2 V Input Range

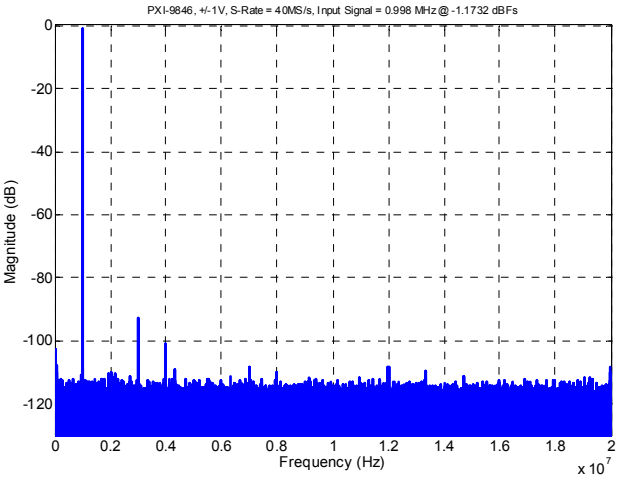

Figure 1-9: PXI-9846 FFT with ±1 V Input Range

Timebase

Specification	Value		
Sample Clock Sources	Internal: onboard oscillator		
	External: CLK IN (front panel SMB connector), PXI STAR, PXI Trigger Bus[0..7], PXI 10MHz, SSI bus		
	PCI/PXI-9816	PCI/PXI-9826	PCI/PXI-9846
Timebase Frequency Range	10 MHz-1 MHz	20 MHz-1 MHz	40 MHz-1 MHz
Sampling Rate Range (24-bit divided counter)	10 MS/s-0.596 S/s	20 MS/s-1.192 S/s	40 MS/s-2.384 S/s
Internal Oscillator Stability	±25 ppm		
CLK IN (external clock from front panel)			
Connector Type	SMB		
Clock Type	Sine wave or square wave		
Input Impedance	50 Ω		
Input Coupling	AC		
Input Range	1VP-P to 2VP-P		
Overvoltage Protection	2.5 V_{P-P}		

Table 1-8: Timebase

Triggering

Specification	Value
Trigger Sources	Software, TRG IO (front panel SMB connector), analog trigger from CH0~CH3, PXI STAR, PXI Trigger Bus[0..7], SSI bus
Trigger Modes	Pre-trigger, Post-trigger, Middle-trigger, Delay-trigger
TRG IO, as input port	
Connector type	SMB
Compatibility	3.3 V LVTTL, 5 V tolerant
Input Level	High threshold (V_{IH}): 2.0 V, minimum Low threshold (V_{IL}): 0.8 V, maximum
Maximum Input Overload	-0.5 V to +5.5 V
Trigger Polarity	Rising edge or falling edge, software program-mable
Minimum Pulse Width	20 ns
TRG IO, as output port	
Connector Type	SMB
Compatibility	3.3 V TTL
Output Level	High threshold (VOH): 2.4V, minimum Low threshold (VOL): 0.2, maximum
Driving Capability	8 mA
Minimum Output Pulse Width	20 ns
Analog Trigger	
Sources	AI channel 0 - 3
Trigger Slope	Rising or falling, software selectable
Trigger Level Range	Full scale input range
Trigger Level Resolution	8-bit, 256 steps in full scale range

Table 1-9: Triggering

Data Storage and Transfer

Specification	Value
Onboard Memory Size	512 MB, share for four channels
Data Transfer	Scatter-gather DMA

Table 1-10: Data Storage and Transfer

Onboard Reference

Specification	Value
Onboard Reference Voltage	5 V
Temperature Drift	±3 ppm/°C
Recommended Warm-up Time	15 minutes

Table 1-11: Onboard Reference

General Information

Specification	Value		
Environment			
Operating Environment	Ambient temperature: 0°C to +55°C for PXI version, 0°C to +50°C for PCI version Relative humidity: 10% to 90%, non-condensing		
Storage Environment	Ambient temperature: -20°C to +85°C Relative humidity: 10% to 90%, non-condensing		
Physical			
PCB Dimension (not including connectors)	PXI version: Single 3U PXI module, 100 mm by 160 mm PCI version: Standard height, half length PCI card, 167.64 mm by 106.68 mm		
PCI Slot Width	1-slot		
PCI Bus Interface			
PCI Signaling	Support 3.3 V and 5 V signaling		
PCI Interface	32-bit, 66 MHz		
Electromagnetic Compatibility			
Emission	EN 55022		
Immunity	EN 55024		
Typical Power Requirements			
	PCI/PXI-9816	PCI/PXI-9826	PCI/PXI-9846
+12 V	0.3 A	0.3 A	0.3 A
+5 V	1.4 A	1.5 A	2.0 A
+3.3 V	0.8 A	0.8 A	0.8 A
Total Power	13.2 W	13.7 W	16.2 W

Table 1-12: General Information

2 Getting Started

This chapter describes the proper installation environment, installation procedures, its package contents and basic information user should be aware of.

NOTE: Diagrams and images of equipment mentioned are used for reference only. Actual system configuration and specs may vary.

2.1 Installation Environment

Whenever unpacking and preparing to install any equipment described in this manual, please refer to the Important Safety Instructions chapter of this manual.

Only install equipment in well lit areas on flat, sturdy surfaces with access to basic tools such as flat and cross head screwdrivers, preferably with magnetic heads as screws and standoffs are small and easily misplaced.

Recommended Installation Tools

- Philips (cross-head_ screwdriver
- Flat-head screwdriver
- Anti-static wrist strap
- Anti-static mat

The PCI/PXI-9816/26/46 contain several electro-static sensitive components that can be easily be damaged by static electricity. The equipment should be handled on a grounded anti-static mat and the operator should wear an anti-static wristband during the unpacking and installation procedure.

Please also inspect the components for apparent damage. Improper shipping and handling may cause damage to the components. Be sure this is no shipping and handling damage on the components before continuing.

CAUTION The equipment must be protected from static discharge and physical shock. Never remove any of the socketed parts except at a static-free workstation. Use the anti-static bag shipped with the product to handle the equipment and wear a grounded wrist strap when servicing.

2.2 Package Contents

Before continuing, check the package contents for any damage and check if the following items are included in the packaging:

- PCI/PXI-9816/26/46 digitizer card
- ADLINK All-in-one CD.
- Software installation guide
- PCI/PXI-9816/26/46 User's Manual.

CAUTION Do not install or apply power to equipment that is damaged or if there is missing/incomplete equipment. Retain the shipping carton and packing materials for inspection. Please contact your ADLINK dealer/vendor immediately for assistance. Obtain authorization from your dealer before returning any product to ADLINK.

2.3 Mechanical Drawing and I/O Connectors

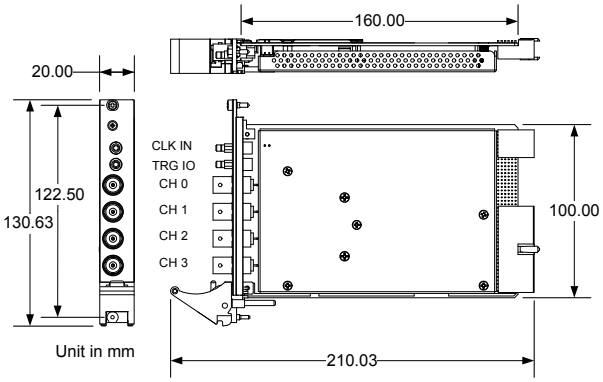

Figure 2-1: PXI-98x6 Mechanical Drawing

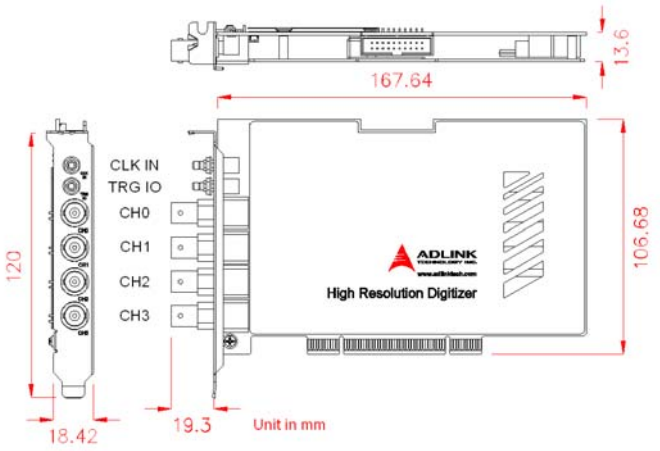

Figure 2-2: PCI-98x6 Mechanical Drawing

The ADLINK PXI-9816/PXI-9826/PXI-9846 is packaged in a Euro-card form factor with PXI specifications measuring 160 mm in length and 100 mm in height (not including connectors). The PCI-9816/9826/9846 is a half-length and standard height PCI form factor. Please refer to above figure for detail dimension.

The connector types and functions are described as follows.

Connector	Direction	Type	Description/Function
CLK IN	Input	SMB	The CLK IN is a 50Ω, AC-coupled external timebase input.
TRG IO	Input Output	SMB	The TRG IO is a bidirectional port for external digital trigger input or output.
CH0	Input	BNC	These channels are for attaching the analog input signals.
CH1			
CH2			
CH3			

Table 2-1: Connector Pin Assignments

2.4 Installing the module

To install the PXI-9816/PXI-9826/PXI-9846 module:

1. Turn off the PXI system/chassis and disconnect the power plug from the power source.
2. Align the module's edge with the card guide in the PXI chassis.
3. Slide the module into the chassis, until resistance is felt from the PXI connector.
4. Push the ejector upwards and fully insert the module into the chassis.
5. Once inserted, a "click" can be heard from the ejector latch.
6. Tighten the screw on the front panel.
7. Power on the PXI system/chassis.

To remove the module, reverse step 2 through 6 above.

To install the PCI-9816/PCI-9826/PCI-9846 module:

1. Turn off your computer
2. Remove the top cover of your computer
3. Select an available PCI slot and remove the bracket-retaining screw and the bracket cover.
4. Line up the PCI digitizer with the PCI slot on the back panel. Slowly push down on the top of the PCI digitizer until its card-edge connector is resting on the slot receptacle.
5. Reinstall the bracket-retaining screw to secure the PCI digitizer to the back panel rail.
6. Restore the computer cover.

2.5 Software Support

ADLINK provides comprehensive software drivers and packages to suit various user approaches to building a system. Aside from programming libraries, such as DLLs, for most Windows-based systems, ADLINK also provides drivers for other application environment such as LabVIEW® and MATLAB®. ADLINK also provides ActiveX component ware for measurement and SCADA/HMI, and breakthrough proprietary software applications.

All software options are included in the ADLINK All-in-One CD.

2.5.1 Driver Support for Windows

DAQPilot

DAQPilot is a driver and SDK with a graphics-driven interface for various application development environments. DAQPilot comes as ADLINK's commitment to provide full support to its comprehensive line of data acquisition products and is designed for the novice to the most experienced programmer.

As a task-oriented DAQ driver, SDK and wizard for Windows systems, DAQPilot helps you shorten the development time while accelerating your learning curve for data acquisition programming.

Figure 2-3: DAQPilot Main Interface

You can download and install DAQPilot at:

http://www.adlinktech.com/TM/DAQPilot.html

DAQMaster

The ADLINK DAQMaster is a smart device manager that opens up access to ADLINK data acquisition and test and measurement products. DAQMaster delivers all-in-one configurations and provides you with a full support matrix to properly and conveniently configure ADLINK Test and Measurement products.

As a configuration-based device manager for ADLINK DAQ cards, DAQMaster enables you to manage ADLINK devices and interfaces, install and upgrade software applications, and manage ADLINK DAQPilot tasks.

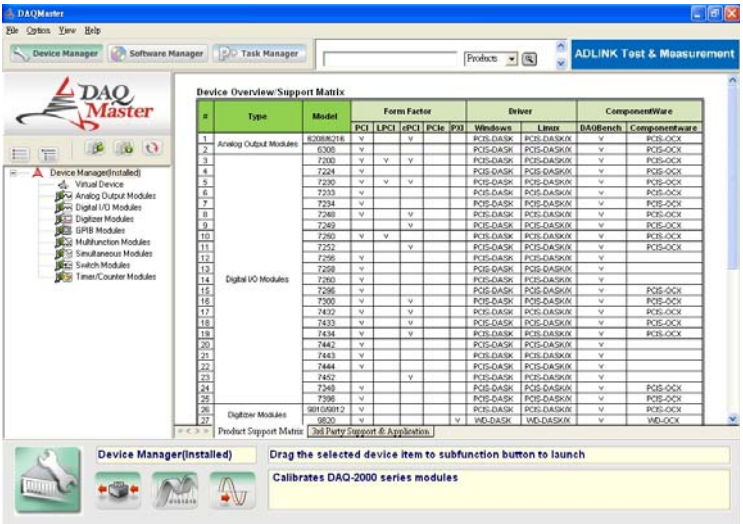

Figure 2-4: DAQMaster Device Manager

2.5.2 WD-DASK (Legacy Drivers and Support)

WD-DASK is composed for advanced 32-bit kernel drivers for customized DAQ application development. WD-DASK enables you to perform detailed operations and achieve superior performance and reliability from your digitizer system. DASK kernel drivers now support the revolutionary Windows Vista OS.

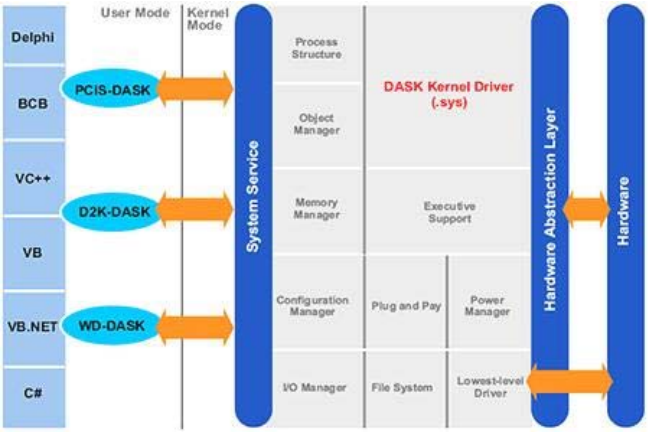

Figure 2-5: Legacy Software Support Overview

3 Operation Theory

The operation theory of the PCI/PXI-9816/26/46 is described in this chapter, including the control and setting of signal sources, trigger sources, trigger modes, data transfers, and synchronizing multiple modules.

3.1 Functional Block Diagram

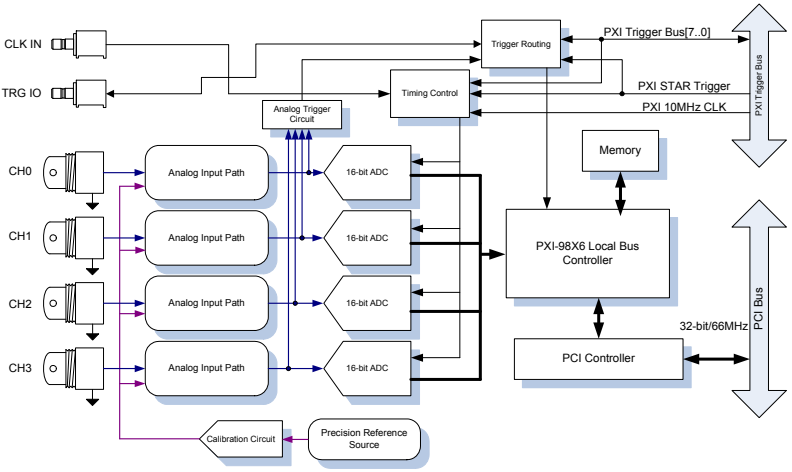

Figure 3-1: PXI-98x6 Functional Block Diagram

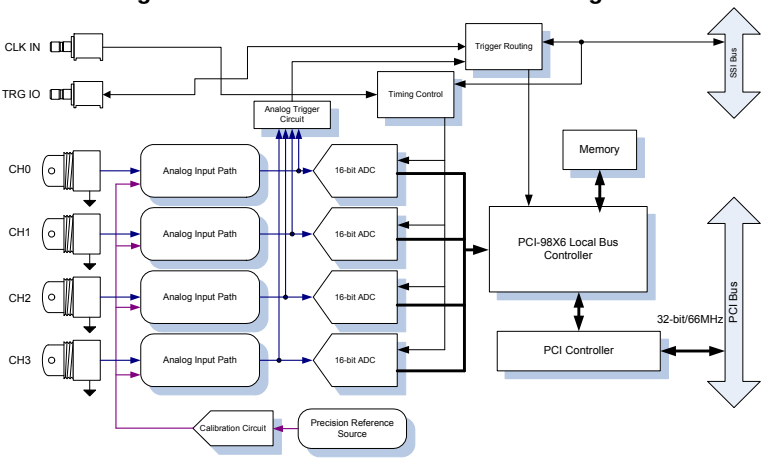

Figure 3-2: PCI-98x6 Functional Block Diagram

3.2 Basic AI Acquisition

In this section, we are going to explain the basic acquisition timing.

3.2.1 Analog Input Path

The following figure shows the block diagram of the single analog input path of a digitizer. Each path provides a choice of 50 Ω input impedance or high impedance. The gain amplifier is optimized for each input range with low noise and high dynamic range. An anti-aliasing filter is also adopted to eliminate high frequency noise. The 16-bit ADC provides not only accurate DC performance but also high signal-to-noise ratio, high spurious-free dynamic range in AC performance.

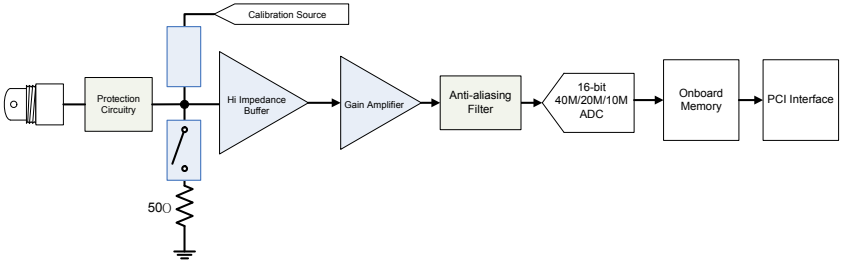

Figure 3-3: Analog Input Signal Block Diagram

3.2.2 Basic Acquisition Timing

The trigger is a signal that starts or stops the acquisition. In post-trigger mode and delay trigger mode, the trigger is used to initiate acquisition. In pre-trigger mode, the trigger is used to stop acquisition. In middle-trigger mode, the trigger is used to inform the acquisition engine to acquire the specific number of data and then stop.

Timebase is a clock that sent to the ADC of each channel and the acquisition engine for essential timing functionality. The source of timebase can be either internal oscillator or external clock generator. Usually the maximum sampling rate of a digitizer is determined by the speed of timebase. However, other sampling rate can be achieved by specifying a scan interval counter. Please refer to Table 3-1 below and Section “3.3.4” on page 32 for more details.

Table 3-1 shows several basic counters required for operating digitizers.

Counter Name	Length	Valid value	Description
ScanIntrv	24-bit	1 - 16777215	**Scan Interval Counter** This counter is a TIMEBASE divider to the achieve equivalent sampling rate of digitizer. The equation is: Sampling rate = TIMEBASE / ScanIntrv The value of TIMEBASE depends on the card type. Take the PCI/PXI-9846 (40 MS/s) as an example, ScanIntrv = 1 results in 40 MS/s and ScanIntrv = 2 results in 20 MS/s, and so on.
DataCnt	29-bit	1 - 536870911	**Data Counter** You can specify the amount of data to be acquired. The digitizer equips 512MB memory to store acquired data.
trigDelayTicks	32-bit	1 - 536870911	**Delay Trigger Counter** The delay trigger counter is used to indicate the time between a trigger event and the start of an acquisition. The unit of a delay count is the period of the TIMEBASE. For PCI/PXI-9816, the unit is 100ns and for PCI/PXI-9846 the unit is 25ns. Refer to section 3.5.4 for more detail.
ReTrgCnt	24-bit	1 - 16777215	**Re-Trigger Counter** The digitizer can enable re-trigger to accept multiple triggers. Refer to section 3.5.5 for more detail.

Table 3-1: Basic Counters

Refer to Figure 3-4 and use post trigger mode as an example. When a trigger is accepted by digitizer, the acquisition engine of the digitizer will begin to acquire data that coming from ADC and store these sampled data to onboard memory. The sampled data is generated continuously at the rising edge of timebase according to the scan interval counter setting. While sampled data reaches customer specified number, in this example is 256, the acquisition ends. Once the acquisition ends, acquisition engine begins to send request to system and transfer data from onboard memory back to system by DMA.

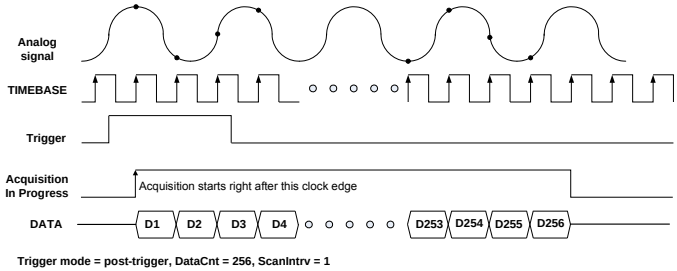

Figure 3-4: Basic Acquisition Timing Of Digitizer

3.2.3 AI Data Format

The following table illustrates the idea transfer characteristics of various input ranges of the PCI/PXI-9816/26/46. The data format of the PCI/PXI-9816/26/46 is straight binary.

Description	Analog Input Range		Digital Code (HEX)
Full-scale Range	±1 V	±0.2 V	
Least significant bit	30.52 µV	6.10 µV	
FSR – 1LSB	0.999969 V	0.199993 V	FFFF
Midscale + 1LSB	30.5 µV	6.10 µV	8001
Midscale	0.0 V	0.0 V	8000
Midscale - 1LSB	-30.5 µV	-6.10 µV	7FFF
-FSR	-1.000 V	-0.200 V	0000

Table 3-2: AI Data Format

3.3 ADC Sampling Rate and TIMEBASE Control

The PXI/PCI-98X6 supports several timebase sources for analog input conversion:

- Internal oscillator
- External clock through front panel
- PXI_STAR (PCI version)
- PXI Trigger Bus[0..7] (PXI version)
- PXI 10M (PXI version)
- SSI (PCI version)

The following diagram shows the timebase architecture of the PXI/PCI-98X6.

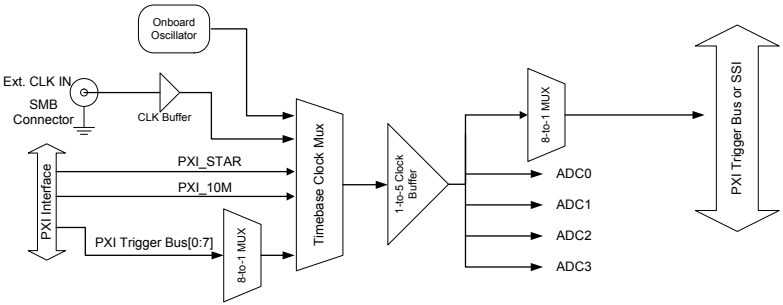

Figure 3-5: PCI/PXI-98x6 Timebase Source and Architecture.

3.3.1 Internal Oscillator

The PCI/PXI-9816/26/46 equips a high stability, low jitter oscillator for the ADCs. The oscillators are 10 MHz, 20 MHz and 40 MHz for PCI/PXI-9816, PCI/PXI-9826 and PCI/PXI-9846, respectively.

3.3.2 External Clock Through Front Panel

When you need a specific timebase in some applications that the onboard oscillator is not achievable, a clock from an external device can replace onboard oscillator. In addition, external timebase also provides a method to synchronize digitizers to other measurement modules by distributing/receiving a common clock to/from multiple modules. The PCI/PXI-9816/26/46 can receive an

external timebase from the front panel connector (CLK IN), PXI STAR or one of the PXI Trigger Bus lines.

You can supply the timebase from external SMB connector CLK IN, which should be a sine wave or square wave signal. This signal is AC coupled with 50 Ω input impedance and the valid input level is from 1 to 2 volts peak-to-peak. Note that the external clock must be continuous for correct ADC operation because of the pipeline architecture of the ADC.

3.3.3 External Clock from PXI Interfaces

The PCI/PXI-9816/26/46 can receive timebase via one of the PXI Trigger Bus lines by software selection. The eight PXI Trigger Bus lines (PXI_TRIG[0..7]) provide inter-module synchronization and communication. Note that this function is only available when the PCI/PXI-9816/26/46 is in a PXI system. It's not supported when PCI/PXI-9816/26/46 is in a CompactPCI system.

When the PCI/PXI-9816/26/46 is plugged into a generic peripheral slot in a PXI system, it can receive timebase from PXI_STAR. The PXI_STAR signal comes from star trigger controller is matched in propagation delay within 1 ns and the delay from star trigger slot to peripheral slot is less than 5 ns. According these hardware features, the PCI/PXI-9816/26/46 can achieve very good synchronization performance when using PXI_STAR as timebase clock source. Note that the function is only available when the PCI/PXI-98x6 is in a PXI system. It's not supported when the PCI/PXI-9816/26/46 is in a CompactPCI system.

3.3.4 Sampling Rate Control

By specifying different scan interval counter (24-bit) value, different sampling rate can be achieved. The following formula determines the ADC sampling rate.

Sampling Rate = TIMEBASE / ScanIntrv

Where ScanIntrv is scan interval counter, value can be 1, 2, 3, 4… 2^{24} - 1.

Refer to Figure 3-6 for detail timing.

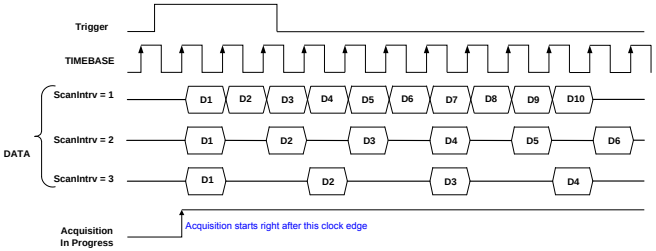

Figure 3-6: Configuring Different Sampling Rate of a Digitizer.

3.3.5 Timebase Exporting

The PCI/PXI-9816/26/46 can export timebase to one of the eight PXI trigger bus lines. By software programming, you can pick up a trigger line to transmit timebase clock. This feature is very useful when synchronize to multiple measurement modules.

3.4 Trigger Sources

In addition to the internal software trigger, the PCI/PXI-9816/26/46 also supports external analog triggers, external digital triggers, PXI_STAR triggers, PXI Trigger Bus[0..7] and SSI bus.. You can configure the trigger source by software command. Please refer to Figure 3.7 for trigger architecture.

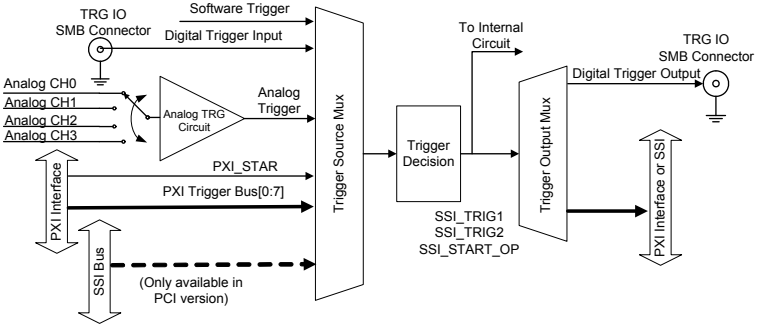

Figure 3-7: PCI/PXI-98x6 Trigger Architecture

3.4.1 Software Trigger

Software trigger is generated by software command. The trigger asserts right after executing specified function calls to begin the operation.

3.4.2 External Digital Trigger

An external digital trigger occurs when a TTL rising edge or a falling edge is detected at the SMB connector TRG IO on the front panel. As illustrated in Figure 3-8, the trigger polarity can be selected by software. Note that the signal level of the external digital trigger signal should be TTL-compatible, and the minimum pulse width is 20 ns.

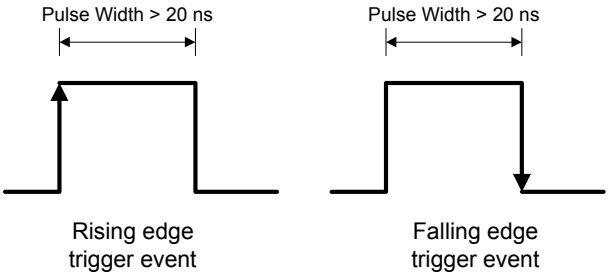

Figure 3-8: External Digital Trigger Polarity and Pulse Width Requirement.

3.4.3 Analog Trigger

You can choose either CH0, CH1, CH2 or CH3 as the trigger signal while using external analog trigger source. The trigger level can be set by software with 8-bit resolution. Please refer to Table 3-3 for the ideal transfer characteristic.

Trigger Level Setting (Hex)	Trigger Voltage (-1V to +1V Range)	Trigger Voltage (-0.2V to +0.2V)
0xFF	0.992V	0.1984V
0xFE	0.984V	0.1968V
---	---	---
0x81	0.0078V	1.56mV
0x80	0V	0V
0x7F	-0.0078V	-1.56mV
---	---	---
0x01	-0.992V	-0.1984V

Table 3-3: Ideal Transfer Characteristics for Analog Triggers

The trigger conditions for analog triggers are illustrated in Figure 3-9 and described as follows:

- Positive-slope trigger: The trigger event occurs when the trigger signal (analog input signal) changes from a voltage that is lower than the specified trigger level to a voltage that is higher than the specified trigger level.
- Negative-slope trigger: The trigger event occurs when the trigger signal (analog input signal) changes from a voltage that is higher than the specified trigger level to a voltage that is lower than the specified trigger level.

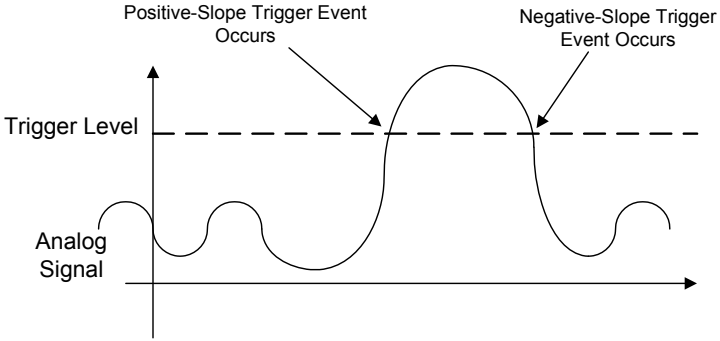

Figure 3-9: Analog Trigger Conditions

3.4.4 PXI STAR Trigger

When you select PXI STAR as the trigger source, the PXI-9816/PXI-9826/PXI-9846 can accept a TTL-compatible digital signal as a trigger signal. The trigger occurs when a rising edge or falling edge is detected at PXI STAR. You can use software to configure the trigger polarity. The minimum pulse width requirement of this digital trigger signal is 20 ns.

3.4.5 PXI Trigger Bus

The PXI-9816/PXI-9826/PXI-9846 utilizes PXI Trigger Bus[0..7] as System Synchronization Interface (SSI). Using the interconnected bus provided by PXI Trigger Bus, you can easily synchronize multiple modules.

When configured as input, the PXI-9816/PXI-9826/PXI-9846 is served as a slave module and can accept three different SSI signals, SSI_TRG1, SSI_TRG2 and SSI_START_OP. When configured as output, the PXI-9816/PXI-9826/PXI-9846 is served as a master module and can output SSI_TRG1, SSI_TRG2 or SSI_START_OP to PXI Trigger Bus. Each signal can be routed from one of the PXI Trigger Bus[0..7] by software programming. For more detail about these signals, please refer to Section “3.7” on page 44.

3.4.6 Trigger Signal Exporting

The PCI/PXI-9816/26/46 can export trigger signals to following connectors/bus: TRG IO on front panel and PXI Trigger Bus[0..7].

The TRG IO on the front panel can also be programmed to output the trigger signal when the trigger source is from software trigger, analog trigger, PXI STAR, or PXI Trigger Bus[0..7]. The timing characteristic is in Figure 3-10.

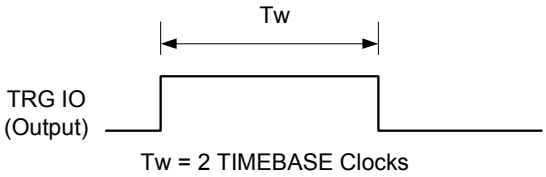

Figure 3-10: TRG IO Output Signal Timing

The PCI/PXI-9816/26/46 utilizes PXI Trigger Bus[0..7] as System Synchronize Interface. When configured as output, the PCI/PXI-9816/26/46 is served as a master module and can output 3 different trigger signals, SSI_TRG1, SSI_TRG2 and SSI_START_OP. You can route these signals to any of PXI Trigger Bus[0..7] signals via software programming.

3.5 Trigger Modes

There four trigger modes working with trigger sources to initiate different data acquisition timing when a trigger event occurs. They are described in this section.

3.5.1 Post-trigger Acquisition

Use post-trigger acquisition when you want to collect data after the trigger event, as illustrated in Figure 3-11.

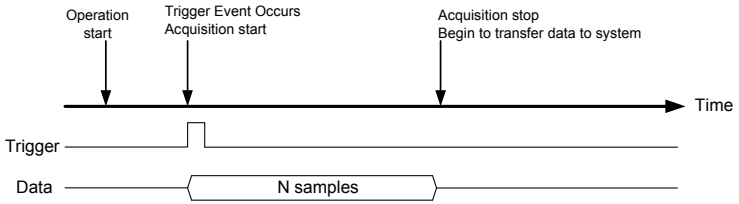

Figure 3-11: Post-trigger Acquisition

3.5.2 Pre-trigger Acquisition

Use pre-trigger acquisition to collect data before the trigger event. The acquisition starts once specified function calls are executed to begin the pre-trigger operation, and it stops when the trigger event occurs.

If the trigger event occurs after the specified amount of data has been acquired, the system only stores the data before the trigger event with specified amount, as illustrated in Figure 3-12.

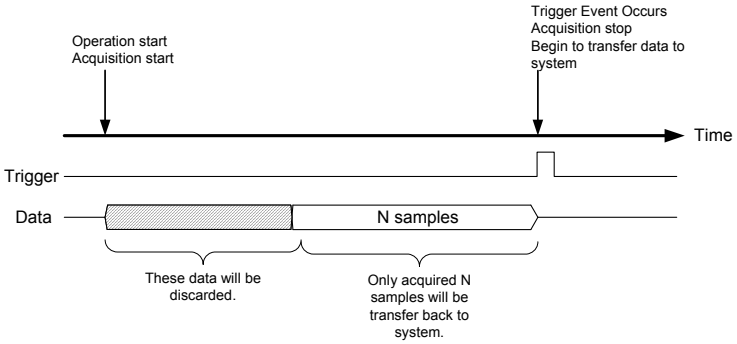

Figure 3-12: Pre-trigger Mode Operation

The trigger event occurs after the specified amount of data has been acquired. However, if the trigger event occurs before the specified amount of data has been acquired, the acquisition engine will ignore the trigger signal until the specified amount of data has been acquired. Refer to Figure 3-13 for an example.

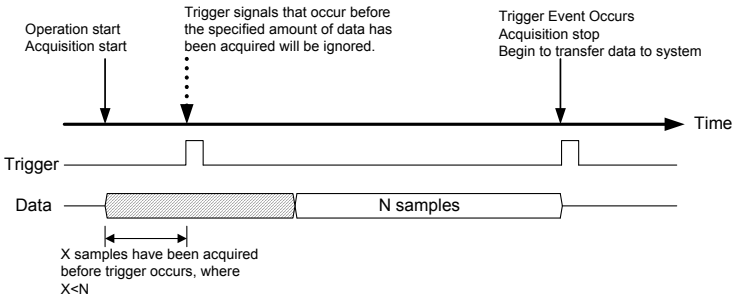

Figure 3-13: Pre-trigger Mode Operation

3.5.3 Middle-trigger Acquisition

Use middle-trigger acquisition when you want to collect data before and after the trigger event. The amount of stored data before and after trigger event can be set individually (M and N samples), as illustrated in Figure 3-14.

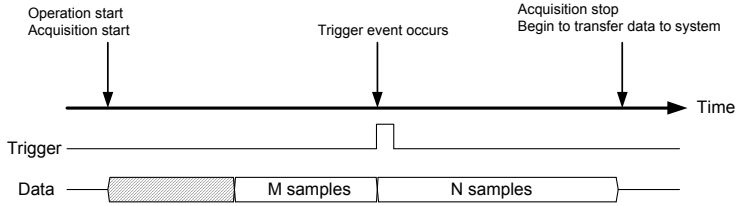

Figure 3-14: Middle-trigger Mode Operation

Please note that trigger event can only accepted when the specified amount of data has been acquired (M samples). If the sampled data is not enough, the trigger event will be ignored.

3.5.4 Delay-trigger Acquisition

Use delay-trigger acquisition to delay the data collection after the trigger event, as illustrated in Figure 3-15. The delay time is specified by a 32-bit counter value so that the maximum delay time is the period of TIMEBASE X (2^{32} - 1), while the minimum delay is the period of timebase.

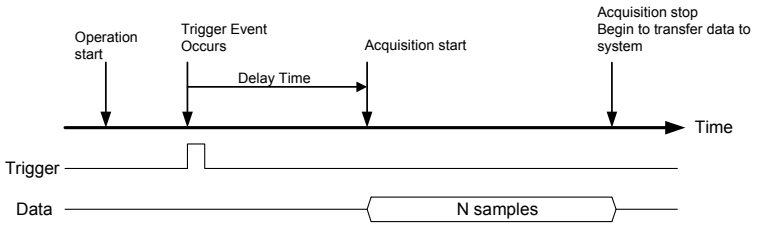

Figure 3-15: Delay-trigger Mode Operation

3.5.5 Post-trigger or Delay-trigger Acquisition with Re-trigger

Use post-trigger or delay trigger acquisition with re-trigger function to collect data after several trigger events, as illustrated in Figure 3-16. You can program the number of triggers then the digitizer will acquire a specific sample data each time a trigger is accepted. All of sampled data will be stored in onboard memory first until all trigger events occurred. Thus the time between last sampled data and next trigger event can be only one clock period of timebase. After the initial setup, the process does not require software intervention.

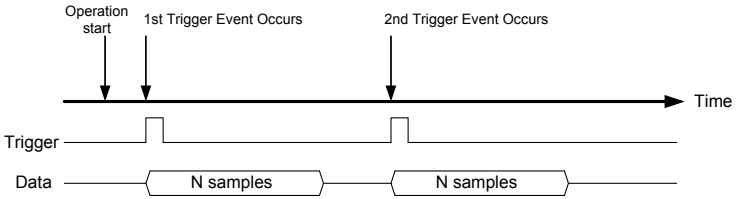

Figure 3-16: Re-trigger Mode Operation.

3.6 Data Transfers

Since the maximum data throughput on the PCI/PXI-9846 (40MS/s * 4 channels *2 Bytes/channel = 320MB/s) is much higher than the 32bit/33MHz PCI-bus bandwidth, samples are acquired into the onboard SDRAM memory before being transferred to the host computer. Since the number of stored samples per acquisition is limited by the amount of on-board memory, the PCI/PXI-9816/26/46 supports maximum 512MB in order to meet application requirements.

Once all the data has been stored in the on-board memory, the data will be transferred to the host computer's memory through bus-mastering DMA.

In a multi-user or multi-tasking OS, like Microsoft Windows, Linux, and so on, it is difficult to allocate a large continuous memory block to do the DMA transfer. Therefore, the PCI/PXI-9816/26/46 provides the function of scatter-gather DMA to link the non-continuous memory blocks into a linked list so that you can transfer very large amounts of data without being limited by the fragment of small size memory, as illustrated in Figure 3-17.

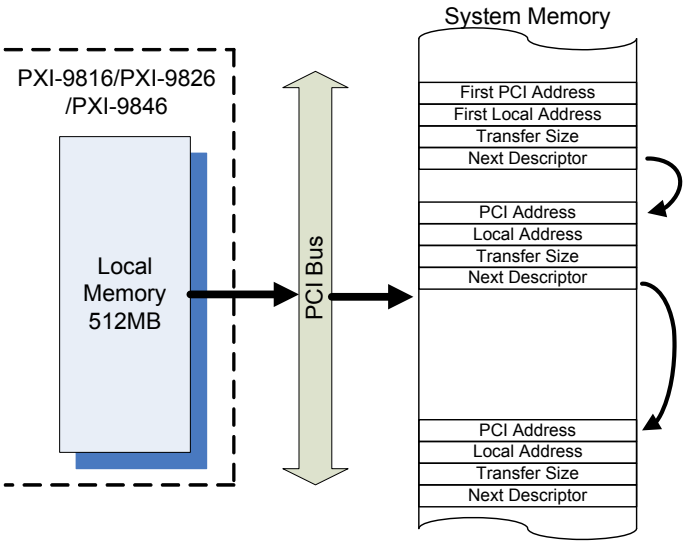

Figure 3-17: Scatter-Gather DMA for Data Transfer

3.7 Synchronizing Multiple Modules

The eight interconnected lines on PXI backplane named as PXI Trigger Bus[0:7] provide a flexible interface for multiple modules synchronization. The PXI-9816/26/46 utilizes the PXI Trigger Bus[0:7] as the System Synchronization Interface (SSI). By providing flexible routing of timebase clock and trigger signals onto PXI Trigger Bus, the PXI-9816/26/46 makes the synchronization between multiple modules easy and simple.

For PCI-9816/26/46, a dedicate connector is served as system synchronization interface. With this interface, PCI-9816/26/46 is capable of achieving multiple module synchronization. Following figure shows the installation of multiple module synchronization.

The bi-directional SSI I/Os provide a flexible connection between modules, which allows one SSI master PCI/PXI-9816/26/46 to output the SSI signals to other slaves modules to receive the signals. Table 3-4 lists the summary of SSI timing signals and the functionalities. Figure 3-18 shows the architecture of SSI. Note that it's not allowed to route different signals onto the same trigger bus line.

SSI Timing Signals	Functionality
SSI_TIMEBASE	Input/output timebase signal through SSI
SSI_TRIG1	Input/output trigger signal through SSI
SSI_TRIG2	Input/output clocked trigger signal through SSI
SSI_START_OP	Input/output the acquisition start signal in pre-trigger or middle-trigger mode

Table 3-4: Summary of SSI timing Signals and the Corresponding Function

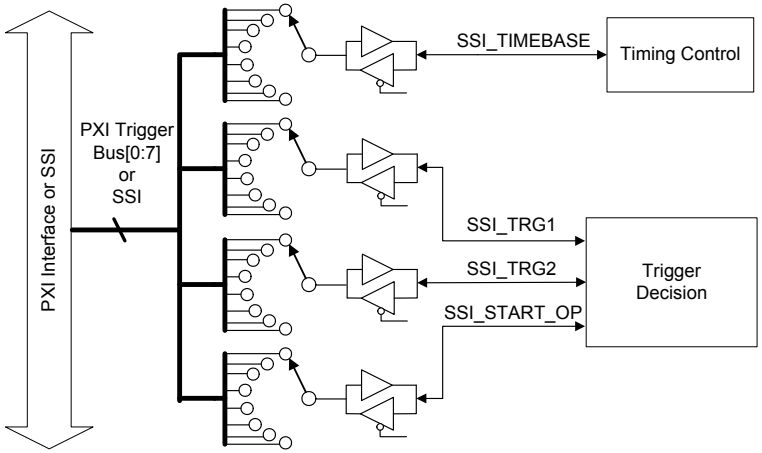

Figure 3-18: SSI Architecture

For PCI-9816/26/46, a dedicate connector is served as system synchronization interface. Refer to Figure 3-19 for the connector position. All the SSI signals are routed to the 20-pin connector from FPGA. With this interface, PCI-9816/26/46 is capable of achieving multiple module synchronization. Users can use ACL-SSI-2/ACL-SSI-3/ACL-SSI-4 cables to synchronize 2, 3, or 4 modules. Please refer to Figure 3-20 for the installation of an ACL-SSI cable.

Note: When powering-up or reseting, the synchronization signals are reset to use internal generated timing signals.

Figure 3-19: SSI Connector Location on the PCI-9816/26/46

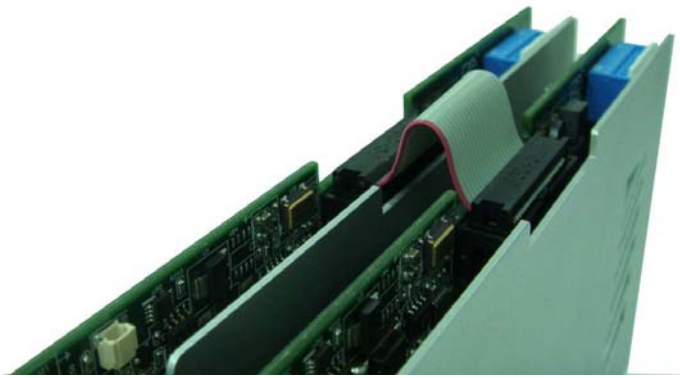

Figure 3-20: Installation of ACL-SSI-2 Cable

CN11	19	17	15	13	11	9	7	5	3	1
	20	18	16	14	12	10	8	6	4	2
PCB										

Signal Name	Direction	Description	Location
SSI_TIMEBASE	Input/Output	Timebase signal through SSI	pin 1
SSI_TRIG1	Input/Output	Trigger signal through SSI	pin 11
SSI_TRIG2	Input/Output	Clocked trigger signal through SSI	pin 9
SSI_START_OP	Input/Output	Acquisition start signal in pre-trigger or middle-trigger mode	pin 7
GND	-	Ground	pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20
NC	-	No Connection	pins 3, 13
Reserved	Input/Output	Reserved for future use	pins 5, 15, 17, 19

Table 3-5: SSI Signal Locations and Pin Definition

3.7.1 SSI_TIMEBASE

As an output, the SSI_TIMEBASE signal outputs the onboard LVTTL timebase through PXI trigger bus.

As an input, the PCI/PXI-9816/26/46 accepts the SSI_TIMEBASE signal to be the source of timebase.

3.7.2 SSI_TRIG1

As an output, the SSI_TRIG1 signal reflects the trigger event signal in an acquisition sequence. You can use the function SSI_SourceConn() to output the SSI_TRIG1 signal.

As an input, the PCI/PXI-9816/26/46 accepts the SSI_TRIG1 signal to be the trigger event source. The signal is configured in the rising edge-detection mode. When selecting the trigger sources of the PCI/PXI-9816/26/46, you can select TRSRC_SSI_1 to set SSI_TRIG1 as the source of trigger event.

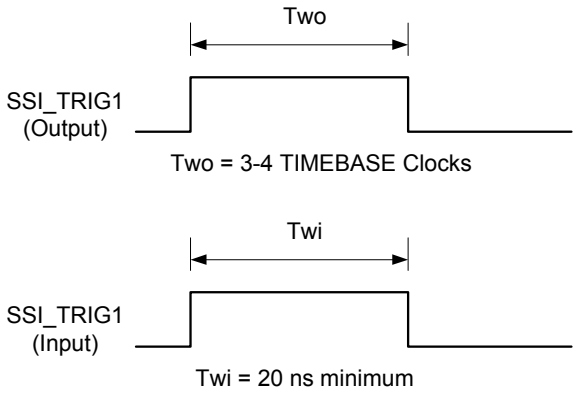

Figure 3-21: SSI_TRIG1 Input and Output Timing Characteristics

3.7.3 SSI_TRIG2 and SSI_START_OP

As an output, the SSI_TRIG2 signal is a clocked SSI_TRIG1 signal by TIMEBASE, as illustrated in Figure 3-22.

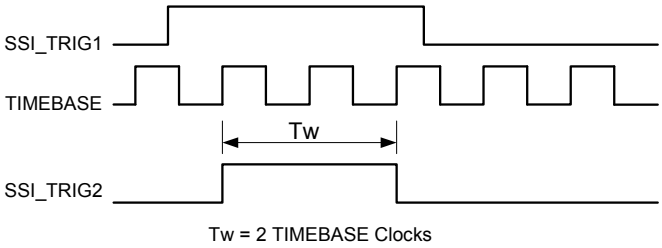

Figure 3-22: SSI_TRIG2 Output Timing

As an input, the PCI/PXI-9816/26/46 accepts the SSI_TRIG2 signal to be the source of a one-clock delayed trigger event. The controller on the PCI/PXI-9816/26/46 will then compensate the one-clock delay if using SSI_TRIG2 as the source of trigger event. The signal is configured in the rising edge-detection mode.

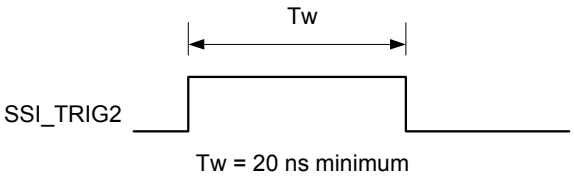

Figure 3-23: SSI_TRIG2 Input Timing Requirement

As an output, the SSI_START_OP signal reflects the operation start signal in a pre-trigger or middle-trigger acquisition sequence. Please refer to Figure 3-12 - Figure 3-14 for the relationship between the operation start signal and the acquisition sequence.

As an input, the PCI/PXI-9816/26/46 accepts the SSI_START_OP signal to be the operation start signal in a pre-trigger or middle-trigger acquisition sequence. The signal is configured in the rising edge-detection mode. Figure 3-24 show the SSI_START_OP signal input and output timing requirements.

For enabling output operations, you can use the function SSI_SourceConn() to output the SSI_TRIG2 and SSI_START_OP signals.

For the input operations, you can select TRSRC_SSI_2 to set SSI_TRIG2 and SSI_START_OP as the source of the trigger event and operation start signal.

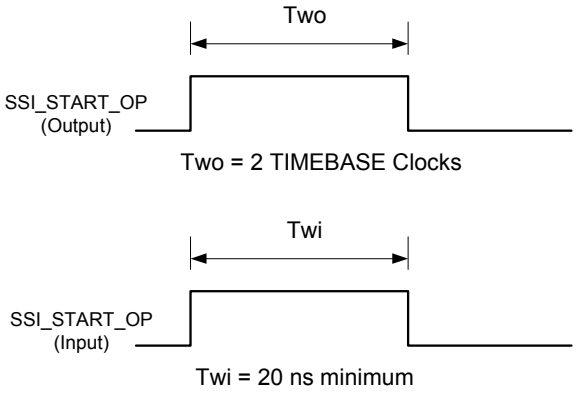

Figure 3-24: SSI_START_OP Output and Input Timing Characteristics

3.7.4 Comparing the Different Trigger Sources from SSI

When selecting TRSRC_SSI_1 as the trigger source input, the signal SSI_TRIG1 reflects the trigger event signal in an acquisition sequence. However, when synchronizing multiple PCI/PXI-9816/26/46 devices, each module may recognize the trigger signal with one-clock time difference because the signal is not related to the timebase.

There is another phenomenon if using TRSRC_SSI_2 in pre-trigger and middle-trigger mode. The operation start signal is generated by a software command so multiple PCI/PXI-9816/26/46 modules don't start the data acquisition simultaneously, which may result in the fact that the amount of stored samples are different if the trigger event occurs before the specified amount of data has been acquired.

When selecting TRSRC_SSI_2 as the trigger source input, SSI_TRIG2 and SSI_START_OP can achieve better synchroniza-

tion between multiple PCI/PXI-9816/26/46 devices. A clocked SSI_TRIG2 can guarantee all PCI/PXI-9816/26/46 devices recognize the trigger event at the same clock edge if they use the same timebase. In pre-trigger and middle-trigger mode, SSI_START_OP guarantees all the PCI/PXI-9816/26/46 devices start the data acquisition at the same time.

3.8 Physical Location of the PXI and PCI Digitizer

3.8.1 Identify PXI Digitizer's Physical Location by Geographic Address

CompactPCI and PXI chassis accommodate slot numbering mechanism based on the definition of Geographical Address pins on its backplane. Users can identify module's physical location by reading back Geographical Address. This is a useful feature especially when multiple modules are installed in one host system. The PXI-9816/26/46 can read back the Geographical Address through software driver. Please refer to software function reference manual for more detail description.

3.8.2 Assign a Board ID to a PCI Digitizer

When users plug two or more PCI-9816/26/46 modules in one computer, board ID provides an effective mechanism for user to identity the specific module. With this method, users can access to specific module in accordance with board ID. The dip switch of board ID is located on the top of the module. Please refer to following figure and table for detail setting.

Please note that users have to assign a unique board ID to each module that are installed in the same computer, otherwise software driver will not allocate correct system resource to these modules. Once users assign identical board ID to different module, please turn off your computer first and then adjust the board ID again. After correct board ID is assigned, then users can power up computer again.

Figure 3-25: The Location of Board ID Switch

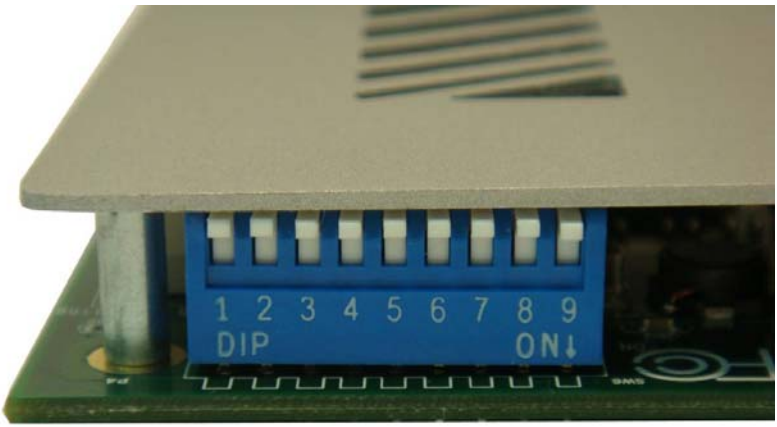

Figure 3-26: Enlargement of Board ID setting.

Note: Only dip switches 1-5 are valid for board ID settings. Dip switches 6- 9 are unused. When a dip switch is switched to 'ON', it represents '1', the opposite direction represents '0'.

Board ID	Switch Number				
	1	2	3	4	5
0	1	1	1	1	1
1	0	1	1	1	1
2	1	0	1	1	1
3	0	0	1	1	1
4	1	1	0	1	1
5	0	1	0	1	1
6	1	0	0	1	1
7	0	0	0	1	1
8	1	1	1	0	1
9	0	1	1	0	1
10	1	0	1	0	1
11	0	0	1	0	1
12	1	1	0	0	1
13	0	1	0	0	1
14	1	0	0	0	1
15	0	0	0	0	1
16	1	1	1	1	0
17	0	1	1	1	0
18	1	0	1	1	0
19	0	0	1	1	0
20	1	1	0	1	0
21	0	1	0	1	0
22	1	0	0	1	0
23	0	0	0	1	0
24	1	1	1	0	0
25	0	1	1	0	0
26	1	0	1	0	0
27	0	0	1	0	0
28	1	1	0	0	0
29	0	1	0	0	0
30	1	0	0	0	0
31	0	0	0	0	0

1: ON

0: OFF

Table 3-6: Board ID Combination Conditions

Important Safety Instructions

Please read and follow all instructions marked on the product and in the documentation before operating the system. Retain all safety and operating instructions for future use.

- Please read these safety instructions carefully.
- Please keep this User's Manual for future reference.
- The equipment should be operated in an ambient temperature between 0 to 50°C.
- The equipment should be operated only from the type of power source indicated on the rating label. Make sure the voltage of the power source is correct when connecting the equipment to the power outlet.
- If the user's equipment has a voltage selector switch, make sure that the switch is set to the proper position for the area. The voltage selector switch is set at the factory to the correct voltage.
- For pluggable equipment, ensure they are installed near a socket-outlet that is easily accessible.
- Secure the power cord to prevent unnecessary accidents. Do not place anything over the power cord.
- If the equipment will not be in use for long periods of time, disconnect the equipment from mains to avoid being damaged by transient overvoltage.
- All cautions and warnings on the equipment should be noted.
- Please keep this equipment away from humidity.
- Do not use this equipment near water or a heat source.
- Place this equipment on a reliable surface when installing. A drop or fall could cause injury.
- Never pour any liquid into the opening, this could cause fire or electrical shock.

- Openings in the case are provided for ventilation. Do not block or cover these openings. Make sure there is adequate space around the system for ventilation when setting up the work area. Never insert objects of any kind into the ventilation openings.
- To avoid electrical shock, always unplug all power and modem cables from the wall outlets before removing covers.
- Lithium Battery provided (real time clock battery)

  "CAUTION - Risk of explosion if battery is replaced by an incorrect type. Dispose used batteries as instructed in the instructions"
- The equipment should be checked by service personnel if one of the following situation arises:
  - The power cord or plug is damaged.
  - Liquid has penetrated the equipment.
  - The equipment has been exposed to moisture.
  - The equipment is not functioning or does not function according to the user's manual.
  - The equipment has been dropped and damaged.
  - If the equipment has obvious sign of breakage.
- Never open the equipment. For safety reasons, the equipment should only be opened by qualified service personnel.